Amendments to the Specification

Please make the following amendments to the specification.

Please replace paragraph 0031 with the following:

[0031] FIG. ~~83~~ 8B is a simplified plot of frequency vs. noise energy for the quantizer of FIG. 8A.

Please replace paragraph 0038 with the following:

[0038] In one embodiment, MUX 21 of FIG. 2 may be placed in the feedback loop of the PLL, i.e., between VCO 20 and PD 10, as shown by MUX ~~31~~ 21 in FIG. 4. The input of the MUX ~~31~~ 21 is driven by a divide-by-K/M circuit 23 to select one out of M inputs of the MUX. In other words, this scheme feeds back the output of the phase shift to PD 10 through the low pass filter 13 and thus smoothes the clock transition when the phase is shifted from 2 phase PH (k) to phase PH (k±1) , resulting in low jitter generation at the output of the VCO. In this embodiment, the jitter energy is ~~futther~~ further reduced by the low pass filter of the PLL.

Please replace paragraph 0039 with the following:

[0039] The above scheme may be enhanced by using various quantizers as illustrated in FIG. 5. The output of the divide-by-Q 43 is quantized by quantizer 44 to drive MUX ~~31~~ 21 selector. A truncator may used as a quantizer, as shown in FIG. 6A. In this scheme, the j MSB bits of the counter are used to drive the MUX ~~31~~ 21 , where 2^j=M. FIG. 6B is a simplified circuit diagram of the modified PLL using the truncator of FIG. 6A. In one embodiment, the quantizer is used in combination with the modified PLL of FIG. 2, where the MUX is not in the feedback loop of the PLL.

Please replace paragraph 0042 with the following:

[0042] FIG. 8A depicts yet an exemplary function of the quantizer circuitry 44. Assuming $2^p = Q$, the output of the divide-by-Q circuit 43 is fed to a ~~quantize~~ quantizer. For this example, an integrator 45 with a transfer function of $Z^{-1}/(1-Z^{-1})$ is used, however, other types of noise shaping blocks may also be used.

Please replace paragraph 0043 with the following:

[0043] Then, p-j output of the integrator is ~~feedback~~ fed back and is ~~subtr:cted~~ subtracted by the k-bit output of the divide-by-Q circuit 43, while j MSB bits of the filter output are truncated and used to control the MUX ~~31~~ 21 in FIG. 8C. This is an example of noise shaping using the well-known Sigma-Delta technique. In a Sigma-Delta technique, noise is shifted in frequency domain. As shown in ~~FIC~~. FIG. 8B, the quantization noise is shifted in frequency domain Although, the noise power may be amplified in this technique, the noise power is shifted to the higher frequency which is reduced significantly by the low pass loop filter 13 of the PLL. FIG. 8C is a simplified circuit diagram of the modified PLL using the integrator of FIG. 8A. In one embodiment, the noise shaping block is used in combination with the modified PLL of FIG. 2, where the MUX is at the output of the VCO.